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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): BUR920030032US1

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Application Number	Filed
10/604,059	June 24, 2003

First Named Inventor: Charles N. Perez

Art Unit	Examiner
2825	Doan, Nghia M.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number **53,352**.
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 ______

/Duane N. Moore/
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May 17, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Perez, et al. Atty. Docket No.: BUR920030032US1

Serial No.: 10/604,059 Group Art Unit: 2825

Filed: June 24, 2003 Examiner: Doan, Nghia M.

For: METHOD OF DISPLAYING A GUARD RING WITHIN AN INTEGRATED CIRCUIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTACHMENT TO PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

This pre-appeal brief request is being submitted together with a Notice of Appeal and is in response to the Office Action mailed March 21, 2007, setting a three-month statutory period for response. Therefore, this request is timely filed. Claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ker, et al. ("Automatic Methodology for Placing the Guard Rings into Chip Layout to Prevent Latchup in CMOS IC's," IEEE, Vol. 1, September 2001, pp. 113-116), hereinafter referred to as Ker. Applicants respectfully traverse these rejections based on the following discussion.

Applicants respectfully traverse these rejections because the rejections contain two clear errors. First, the references miss the claim element of displaying logic devices and a guard ring symbolically and schematically in a single integrated display. Secondly, the references miss the claim element of displaying a guard ring within a hierarchical integrated circuit design, wherein the hierarchical integrated circuit design has a parameterized cell and at least one guard ring.

A. Missing Claim Element – displaying logic devices and a guard ring symbolically and schematically in a single integrated display (independent claims 1, 13, and 25).

As shown in FIG. 14 of Applicants' disclosure, item 141 illustrates logic devices displayed schematically; item 142 illustrates a guard ring displayed symbolically; and, item 140 illustrates a combination of item 141 and 142; i.e., the logic devices and guard ring are displayed symbolically and schematically in a single integrated display.

To the contrary, Ker does not provide a single integrated display that has *both* symbolic and schematic representations of a guard ring and logic devices. Instead, Ker merely displays "layout views" of component "shapes", wherein the layout views lack schematics. As more fully discussed below, referencing FIG. 4 of Ker, the Office Action argues that the "layout of circuit design … must be constructed from a schematic". However, Applicants submit that such a schematic is not *displayed in combination* with the layout view "in a single integrated display". As further discussed below, although the Office Action argues that FIGS. 1-3 of Ker display schematics, FIGS. 1-3 do not provide a *single* integrated display that has *both* schematic *and symbolic* representations of a guard ring and logic devices as required by Applicants' claims.

The Office Action argues that FIGS. 4(a) and 4(b) of Ker disclose displaying logic devices and a guard ring symbolically and schematically in a single display (Office Action, p. 3, item. 5). Applicants respectfully traverse this rejection and submit that FIGS. 4(a) and 4(b) of Ker do not disclose displaying logic devices and a guard ring *schematically*. FIGS. 4(a) and 4(b) of Ker do not illustrate the functional device components schematically; instead, "layout views" showing component "shapes" are displayed *without schematics*.

Specifically, as provided in page 114, column 1, section 2.1 of Ker, to provide the connection from the power lines to the guard rings, a cell called as "instance" was setup in a cell library. The "shapes of such instances in different CMOS processes are shown in Fig. 4(a) and 4(b)". Further, the Figure description on page 114, column 2, describes "Layout of the instances". However, FIGS. 4(a) and 4(b) do not display the instances symbolically *and schematically*. FIGS. 4(a) and 4(b) lack a schematic representation of

the guard ring and a schematic representation of the logic devices. The Office Action argues that the instances of FIGS. 4(a) and 4(b) "must be constructed from a schematic" (Office Action, p. 7, para. 1). However, such a schematic is not displayed in FIGS. 4(a) and 4(b) in combination with a symbolic representation of the guard ring and logic devices in a single integrated display. Applicants further note that the circuit illustrated in Fig. 1(b) is not displayed to the user in a display component.

In addition, the Office Action argues that schematics are shown in FIGS. 1-3 of Ker (Office Action, p. 7, para. 1). The fact that multiple figures are referenced supports Applicants' position that logic devices and the guard ring are not displayed in a *single integrated* display. Specifically, the Office Action must reference three *different* figures to illustrate schematic displays and symbolic displays. The Office Action is unable to point to a *single* figure that has *both* schematic *and* symbolic representations of the guard ring and logic devices displayed in a *single integrated* display. To the contrary, as claimed and illustrated in FIG. 14 of Applicants' disclosure, item 140 displays logic devices and a guard ring *both* symbolically *and* schematically in a *single integrated* display.

Accordingly, Applicants submit that unlike the claimed invention, Ker does not disclose displaying logic devices and the guard ring symbolically and schematically in a single display. Instead, "layout views" showing component "shapes" are displayed in Ker without schematics. Therefore, it is Applicants' position that Ker misses the claimed element of "displaying said logic devices and said guard ring symbolically and schematically in a single integrated display" as defined in independent claims 1, 13, and 25.

B. Missing Claim Element – displaying a guard ring within a hierarchical integrated circuit design, wherein the hierarchical integrated circuit design has a parameterized cell and at least one guard ring (independent claim 13).

As discussed in paragraph 0048 of Applicants' disclosure, FIG. 5 is a flowchart that illustrates that the invention first identifies the type of circuit (and the type of ESD protection) 50. This allows the invention to create a parameterized cell (P-cell) 51. The invention then selects the appropriate type of guard ring and places the guard ring within

the P-cell 52. *The combined guard ring and P-cell are produced and can be used in a hierarchical circuit design 53.* As further discussed in paragraph 0056 of Applicants' disclosure, FIG. 13 illustrates a hierarchical structure used for the graphical, circuit schematic, or symbol hierarchy. In FIG. 13, *the guard ring P-cell 131 and hierarchical ESD P-cell 132 are combined to form the ESD guard ring hierarchical design 130.*

Moreover, as discussed in paragraph 0051 of Applicants' disclosure, FIG. 7 is a graphical illustration of an input node ESD P-cell that can be used in a hierarchical design. This *parameterized cell* includes voltage lines VDD 70 and VSS 72 P+/N- well diodes 71 that are positioned between the stretch lines 73. This parameterized cell can be auto-generated and actually contains two primitive parameterized (twin diodes). FIG. 8 illustrates the same structure as that shown in FIG. 7 and includes the *guard ring 80*. In this implementation, the new parameterized cell is modified in that it is now contain all the data information of the parameterized cell guard as well as the ESD parameterized cell.

To the contrary, nothing within Ker discloses the claimed (claim 13) hierarchical integrated circuit design having a parameterized cell and a guard ring. Instead, Ker merely discloses an integrated circuit design having guard rings. Although the Office Action argues that Ker teaches the use of double guard rings (Office Action, p. 4, item 6), nothing within Ker discloses a hierarchical integrated circuit design including such guard rings and a parameterized cell.

In support of its arguments, the Office Action references FIGS. 4(a) and 4(b) of Ker, wherein the Office Action asserts that Ker discloses multiple guard rings. However, the "layout of the instances" shown in FIGS. 4(a) and 4(b) of Ker does not include a hierarchical integrated circuit design. Moreover, the "layout of the instances" shown in FIGS. 4(a) and 4(b) of Ker does not include a parameterized cell. Therefore, it is Applicants' position that Ker fails to teach or suggest the claimed feature of "displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and said at least one guard ring" as defined by independent claim 13.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: May 17, 2007

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